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10/600,171	06/19/2003	Koji Suzuki	YKI-0132	9732

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Michael A. Cantor, Esq.
CANTOR COLBURN LLP
55 Griffin Road South
Bloom field, CT 06002

EXAMINER	
ORTIZ, EDGARDO	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/600,171	SUZUKI, KOJI
	Examiner	Art Unit
	Edgardo Ortiz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art figures 1A-1B and their description in pages 1-4 of the instant application in view of Fukuda (U.S. Patent No. 5,880,035). With regard to Claim 1, Applicant's admitted prior art discloses a method for manufacturing a thin-film transistor, comprising the steps of: forming a semiconductor film (23) above a substrate (21), forming a gate insulating film (24) to cover the semiconductor film, forming a gate electrode (25) on the gate insulating film (24), wherein the gate electrode (25) comprises a refractory metal (Mo) (see page 1, lines 23-25 of the instant application) forming a source region (23s) and a drain region (23d) in the semiconductor film and forming an interlayer insulating film (26) on the gate electrode (25), wherein in the formation of the gate electrode (25), an electrode material layer is layered on the gate insulating film (24); a mask pattern is formed on the electrode material layer (see page 3, lines 1-3 of the instant application); an etching process is applied in which the electrode material layer is etched using gas containing fluorine or gas containing a mixture of fluorine and oxygen (see page 3, lines 3-6 of the instant application), and with the mask pattern as a mask to a degree wherein a portion of the electrode material layer remains.

Applicant's admitted prior art fails to disclose the claimed second etching process using a gas containing a mixture of chlorine and oxygen. However, Fukuda discloses a dry-etching method for a gate electrode comprising layers (2, 3) wherein layer (2) comprises a refractory metal (column 5, lines 58-60). The dry-etching method includes a first etching step wherein the gas used in said first etch step is SF_6 and a second etch step wherein the gas used is Cl_2/O_2 (see column 3, lines 28-33 and column 6, lines 1-21 and 41-42). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the process as taught by Applicant's admitted prior art to include the claimed second etching process, which uses a gas containing a mixture of chlorine and oxygen, as suggested by Fukuda, in order to provide a dry-etching method that enables higher productivity and a higher yield without damaging the substrate or a gate oxide film (column 2, lines 45-50).

With regard to Claim 2, Applicant's admitted prior art discloses that the source region (23s) and the drain region (23d) are formed by, doping impurities into the semiconductor film (23) through the gate insulating film (24) (see page 1, lines 25-28 of the instant application).

With regard to Claim 3, Applicant's admitted prior art discloses a gate insulating film (24) that is obtained by layering a SiN film and a SiO2 film or by forming one of the SiN film and SiO2 film (see page 1, line 22 of the instant application).

With regard to Claim 4, Applicant's admitted prior art discloses a source region (23s) and a drain region (23d) formed by doping impurities into the semiconductor film (23) through the gate

insulating layer (24) (see page 1, lines 25-28 of the instant application), and the gate insulating film is obtained by layering a SiN film and a SiO2 film or by forming one of the SiN film and SiO2 film (see page 1, line 22 of the instant application).

With regard to Claim 5, Applicant's admitted prior art discloses a first etching process which is produced by mixing fluorine-based gas and oxygen-based gas in an approximately equal volume ratio (see page 3, lines 1-6 of the instant application).

With regard to Claim 6, Applicant's admitted prior art discloses a method for manufacturing a thin-film transistor, comprising the steps of: forming a semiconductor film (23) above a substrate (21), forming a gate insulating film (24) to cover the semiconductor film, forming a gate electrode (25) on the gate insulating film, forming a source region (23s) and a drain region (23d) within the semiconductor film (23) and forming an interlayer insulating film (26) on the gate electrode (25), wherein in the formation of the gate electrode (25) an electrode material layer is layered on the gate insulating film (24); a mask pattern is formed on the electrode material layer (see page 3, lines 1-3 of the instant application) and an etching process applied to the electrode material layer with the mask pattern of a resist material as a mask, wherein the gate electrode (25) has a tapered shape which becomes narrower toward the upper surface (see figure 1B).

Applicant's admitted prior art fails to disclose the claimed first and second etching processes with different etching selection ratios. However, Fukuda discloses a dry-etching method for a gate electrode comprising layers (2, 3) wherein layer (2) comprises a refractory metal (column 5,

lines 58-60). The dry-etching method includes a first etching step wherein the gas used in said first etch step is SF_6 and a second etch step wherein the gas used is Cl_2/O_2 (see column 3, lines 28-33 and column 6, lines 1-21 and 41-42). It is noted that since Fukuda discloses the same gases, SF_6 and Cl_2/O_2, for the first and second etching steps respectively, these gases have the same characteristics of selection ratio as claimed by Applicant. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the process as taught by Applicant's admitted prior art to include disclose the claimed first and second etching processes with different etching selection ratios, as suggested by Fukuda, in order to provide a dry-etching method that enables higher productivity and a higher yield without damaging the substrate or a gate oxide film (column 2, lines 45-50).

With regard to Claims 21 and 22, Applicant's admitted prior art teaches a gate electrode (25) having a single layer structure (see figure 1B of the instant application).

2. Claims 7-15 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art figures 1A-1B and their description in pages 1-4 of the instant application in view of Fukuda (U.S. Patent No. 5,880,035) and further in view of Paranjpe et al. (U.S. Patent No. 5,580,385). With regard to Claim 7, Applicant's admitted prior art and Fukuda essentially disclose the claimed invention, but fail to disclose the claimed inductively-coupled plasma apparatus. However, Paranjpe discloses a method for incorporating an inductively coupled plasma source in a plasma processing chamber, wherein the inductively-coupled plasma source comprises an antenna (14) powered by at least one RF power supply (40) through at least

one RF matching network (42) and a plasma-formation region (30). See figure 1. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the process as taught by Applicant's admitted prior art to include the claimed the claimed inductively-coupled plasma apparatus instead of the ECR plasma etching system of Fukuda, in order to provide a plasma processing chamber with a source that has substantially lower instrinsic plasma potentials and achieve substantially higher ionization efficiency (column 1, lines 31-40) and operates over a pressure range that is more compatible with process requirements (column 1, lines 48-50).

With regard to Claim 8, Applicant's admitted prior art discloses a semiconductor film (23) that is formed above a substrate (21) and an electrode material (25) that is formed above the semiconductor film (23) (see figures 1A-1B and page 1, lines 14-29 to page 4, lines 1-14 of the instant application).

With regard to Claim 9, Applicant's admitted prior art discloses a gate insulating film (24) that is formed on a semiconductor film (23) and an electrode material layer (25) formed on the gate insulating film (24) (see figures 1A-1B and page 1, lines 14-29 to page 4, lines 1-14 of the instant application).

With regard to Claim 10, Applicant's admitted prior art discloses a process step of forming a gate electrode (25), wherein the gate electrode has a tapered shape (see figures 1A-1B and page 1, lines 14-29 to page 4, lines 1-14 of the instant application).

With regard to Claim 11, Applicant's admitted prior art teaches an etching process which is produced by mixing fluorine-based gas and oxygen-based gas (page 3, lines 1-5 of the instant application). However, Applicant's admitted prior art fails to teach a second etching process, which uses a gas containing a mixture of chlorine and oxygen. However, Fukuda discloses a dry-etching method for a gate electrode comprising layers (2, 3) wherein layer (2) comprises a refractory metal (column 5, lines 58-60). The dry-etching method includes a first etching step wherein the gas used in said first etch step is SF_6 and a second etch step wherein the gas used is Cl_2/O_2 (see column 3, lines 28-33 and column 6, lines 1-21 and 41-42). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the process as taught by Applicant's admitted prior art to include the claimed second etching process, which uses a gas containing a mixture of chlorine and oxygen, as suggested by Fukuda, in order to provide a dry-etching method that enables higher productivity and a higher yield without damaging the substrate or a gate oxide film (column 2, lines 45-50).

With regard to Claim 12, Applicant's admitted prior art teaches a semiconductor film (23) that is formed above a substrate (21) and an electrode material (25) that is formed above the semiconductor film (see figures 1A-1B and page 1, lines 14-29 to page 4, lines 1-14 of the instant application).

With regard to Claim 13, Applicant's admitted prior art teaches a gate insulating film (24) that is formed on a semiconductor film (23) and an electrode material layer (25) formed on the gate

insulating film (see figures 1A-1B and page 1, lines 14-29 to page 4, lines 1-14 of the instant application).

With regard to Claim 14, Applicant's admitted prior art teaches a gate insulating film (24) that is obtained by layering a SiN film and a SiO2 film or by forming one of the SiN film and SiO2 film (see page 1, line 22 of the instant application).

With regard to Claim 15, Applicant's admitted prior art teaches a process step of forming a gate electrode (25), wherein the gate electrode has a tapered shape (see figures 1A-1B and page 1, lines 14-29 to page 4, lines 1-14 of the instant application). However, Applicant's admitted prior art fails to teach a second etching process. However, Fukuda discloses a dry-etching method includes a first etching step wherein the gas used in said first etch step is SF_6 and a second etch step wherein the gas used is Cl_2/O_2 (see column 3, lines 28-33 and column 6, lines 1-21 and 41-42). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the process as taught by Applicant's admitted prior art to include the claimed second etching process, which uses a gas containing a mixture of chlorine and oxygen, as suggested by Fukuda, in order to provide a dry-etching method that enables higher productivity and a higher yield without damaging the substrate or a gate oxide film (column 2, lines 45-50).

With regard to Claim 23, Applicant's admitted prior art teaches a gate electrode (25) having a single layer structure (see figure 1B of the instant application).

Response to Arguments

3. Applicant's arguments with respect to claims 1-15 and 21-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O.
A.U. 2815
6/6/05

TOM THOMAS
SUPERVISORY PATENT EXAMINER